IN THE ABSTRACT

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ABSTRACT

The present invention comprises a clamp circuit (104) comprised of a first transistor (111), a second transistor (112), a voltage divider circuit and a delay circuit (105) comprised of a fourth transistor (114), a fifth transistor (115), a sixth transistor (116) and a seventh transistor (117) and a fifth resistor (125), operable to keep the signals at the EEPROM input nodes (131) and (132) of a data cell, such as an EEPROM cell below a certain voltage threshold, preferable below 10 volts.